



# V103

## TRIPLE 10-BIT LVDS TRANSMITTER FOR VIDEO

### General Description

The V103 LVDS display interface transmitter is primarily designed to support pixel data transmission between a video processing engine and a digital video display. The data rate supports up to SXGA+ resolutions and can be used in Plasma, Rear Projector, Front Projector, CRT and LCD display applications. It can also be used in other high-bandwidth parallel data applications and provides a low EMI interconnect over a low cost, low bus width cable up to several meters in length.

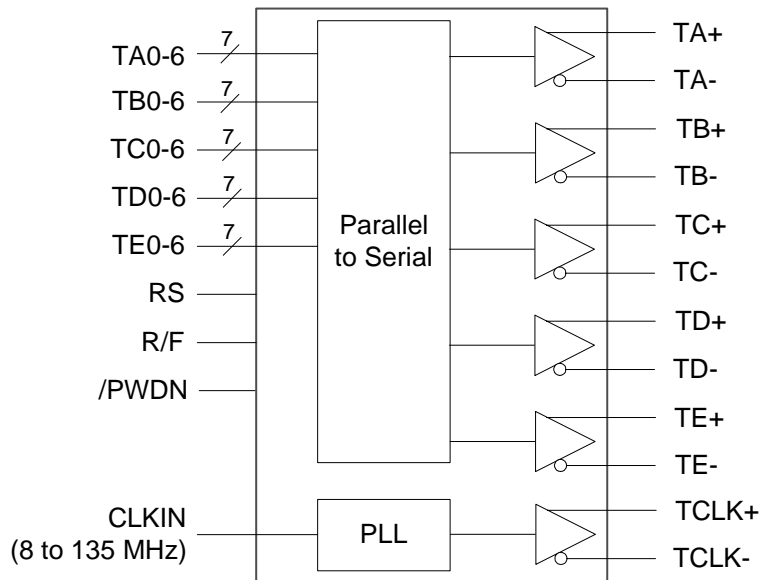
The V103 converts 35 bits of CMOS/TTL data, clocked on the rising or falling edge of an input clock (selectable), into six LVDS (Low Voltage Differential Signaling) serial data stream pairs. In video applications the 35 bits is normally divided into 10 bits for each R, G and B channel and 5 control bits.

When combined with the V104 LVDS display interface receiver, the V103 + V104 combination provides a 35-bit wide, 90 MHz transport. The rate of each LVDS channel is 630 Mbps for a 90MHz data input clock, 945 Mbps for 135MHz.

### Features

- Pin compatible with THine THC63LVD103
- Wide pixel clock range: 8 - 135 MHz
- Supports a wide range of video and graphics modes including VGA, SVGA, XGA, SXGA, SXGA+, NTSC, PAL, SDTV, and HDTV up to 1080I or 720P
- Internal PLL requires no external loop filter
- Selectable rising or falling clock edge for data alignment
- Compatible with Spread Spectrum clock source
- Reduced LVDS output voltage swing mode (selectable) to minimize EMI
- CMOS/TTL data inputs can be configured for reduced input voltage swing
- Single 3.3 V supply
- Low power consumption CMOS design
- Power down mode
- 64-pin TQFP lead free package

### Block Diagram

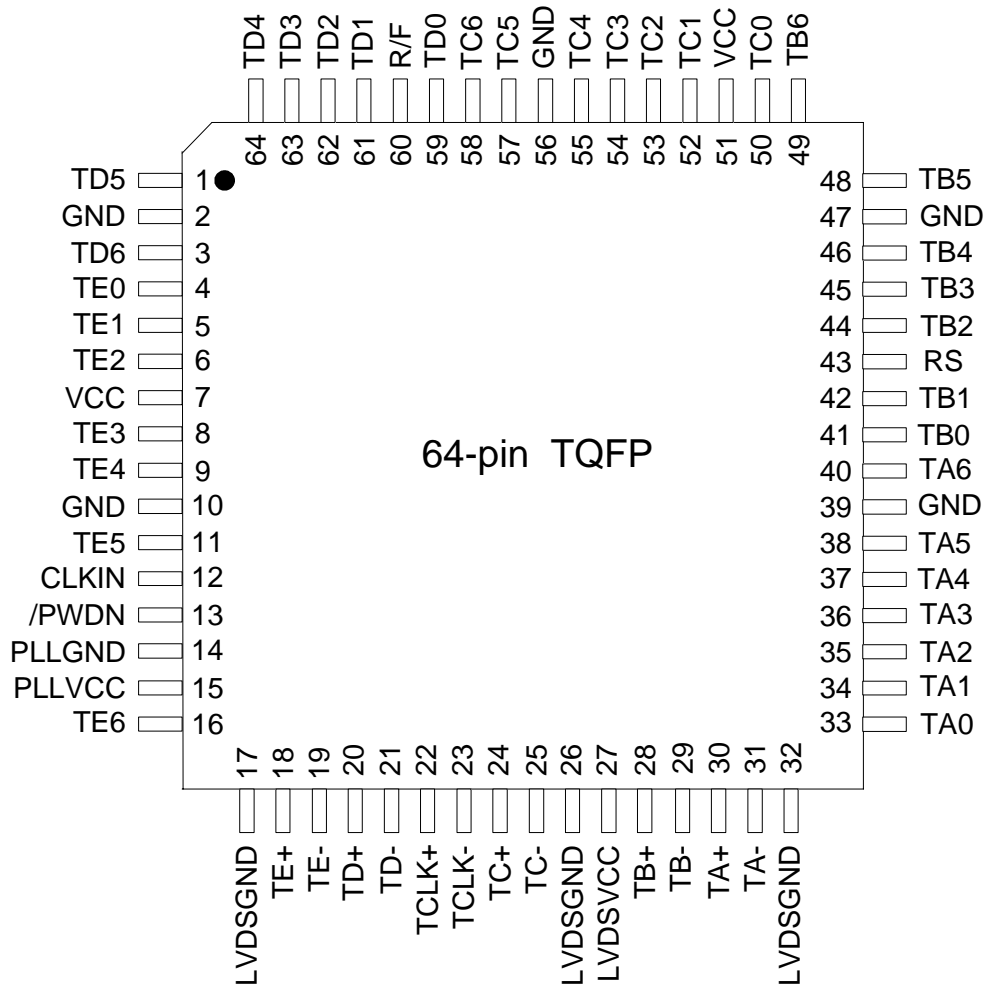


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### Pin Assignment





## Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
30, 31	TA+, TA-	LVDS OUT	LVDS Serial Data Output Pairs
28, 29	TB+, TB-		
24, 25	TC+, TC-		
20, 21	TD+, TD-		
18, 19	TE+, TE-		
22, 23	TCLK+, TCLK-	LVDS OUT	LVDS Reference Clock Output Pair
33, 34, 35, 36, 37, 38, 40	TA0 ~ TA6	IN	CMOS/TTL (or small signal) Data Bit Inputs
41, 42, 44, 45, 46, 48, 49	TB0 ~ TB6		
50, 52, 53, 54, 55, 57, 58	TC0 ~ TC6		
59, 61, 62, 63, 64, 1, 3	TD0 ~ TD6		
4, 5, 6, 8, 9, 11, 16	TE0 ~ TE6		
13	/PWDN	IN	High: Normal device operation Low: Power down; all outputs become high impedance
43	RS	IN	Voltage level on this pin sets LVDS output swing voltage and data input swing voltage; refer to the table at the bottom of this page.
60	R/F	IN	Input Clock triggering edge select. High: Rising edge; Low: Falling edge.
51, 7	VCC	Power	Power supply pins for TTL inputs and digital circuitry.
12	CLKIN	IN	Clock Input.
2, 10, 39, 47, 56	GND	Ground	Ground pins for TTL inputs and digital circuitry.
27	LVDSVCC	Power	Power supply pins for LVDS outputs.
17, 26, 32	LVDSGND	Ground	Ground pins for LVDS outputs.
15	PLLVCC	Power	Power supply pin for PLL circuitry.
14	PLLGND	Ground	Ground pin for PLL circuitry.

### RS Input Voltage Configuration to set LVDS Output Swing and Data Input Swing

RS Input Voltage	LVDS Output Swing	CMOS/TTL Input Configuration (Input Voltage Swing)
VCC	350 mV	Standard Configuration <sup>1</sup>
0.6 ~ 1.4 V (VREF <sup>1</sup> )	350 mV	Small Input Swing Configuration <sup>1</sup>
GND	200 mV	Standard Configuration <sup>1</sup>

Note 1: Refer to DC Electrical Characteristics.





## External Components

Decoupling capacitors should be used for all power pins. The V103 requires no other external components.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the V103. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VCC	-0.3 V to +4.0 V
CMOS/TTL Input Voltage	-0.3 V to VCC+0.3 V
CMOS/TTL Output Voltage	-0.3 V to VCC+0.3 V
LVDS Driver Output Voltage	-0.3 V to VCC+0.3 V
Storage Temperature	-55 to +150°C
Junction Temperature	120°C
Soldering Temperature (10 seconds)	260°C
Maximum Power Dissipation @ 25°C	1.0 W

## Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	°C
Power Supply Voltage (measured in respect to GND)	+3.0	+3.3	+3.6	V



**DC Electrical Characteristics**

VDD=3.3 V ±10%, Ambient temperature 0 to +70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
<b>CMOS/TTL Inputs, Standard Configuration</b>						
Input High Voltage	V <sub>IH</sub>	RS=VCC or GND	2.00		VCC	V
Input Low Voltage	V <sub>IL</sub>	RS=VCC or GND	GND		0.80	V
Input Current	I <sub>INC</sub>	0V ≤ VIN ≤ VCC			±10	μA
<b>CMOS/TTL Inputs, Small Input Swing Configuration</b>						
Max Input Swing Voltage	V <sub>DDQ</sub> <sup>1</sup>	V <sub>REF</sub> = V <sub>RS</sub> = V <sub>DDQ</sub> /2	1.2	V <sub>DDQ</sub> /2	2.8	V
Input Reference Voltage into pin RS	V <sub>REF</sub>					
High Level Input Voltage (for small input swing condition)	V <sub>SH</sub> <sup>2</sup>	V <sub>REF</sub> =V <sub>DDQ</sub> /2	V <sub>DDQ</sub> /2 +0.1V			V
Low Level Input Voltage (for small input swing condition)	V <sub>SL</sub> <sup>2</sup>	V <sub>REF</sub> =V <sub>DDQ</sub> /2			V <sub>DDQ</sub> /2 -0.1V	V

Note 1: V<sub>DDQ</sub> voltage defines the max voltage of the small swing input and is not an actual input into the device.

Note 2: Small input swing voltage is applied to TA[6:0], TB[6:0], TC[6:0], TD[6:0], TE[6:0], and CLKIN.

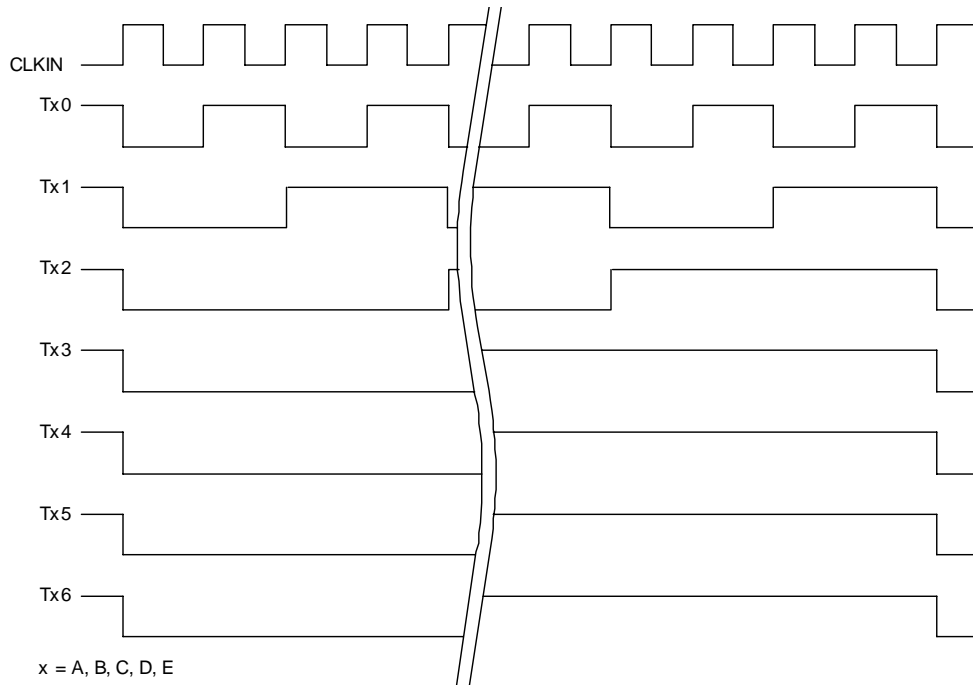
<b>LVDS Transmitter DC Specifications</b>						
Differential Output Voltage, R <sub>L</sub> = 100Ω	V <sub>OD</sub>	Normal swing RS = VCC	250	350	450	mV
		Reduced swing RS = GND	100	200	300	mV
Change in V <sub>OD</sub> Between Complimentary Output States	DV <sub>OD</sub>	RL = 100Ω			35	mV
Common Mode Voltage	V <sub>OC</sub>		1.125	1.250	1.375	V
Change in V <sub>OC</sub> Between Complimentary Output States	DV <sub>OC</sub>				35	mV
Output Short Circuit Current	I <sub>OS</sub>	V <sub>OUT</sub> = 0V, RL = 100Ω			-24	mA
Output Tri-State Current	I <sub>OZ</sub>	/PWDN = 0V, V <sub>OUT</sub> = 0V to VCC			±10	μA

<b>Supply Current</b>						
Transmitter Supply Current	I <sub>TCCG</sub>	R <sub>L</sub> = 100Ω, C <sub>L</sub> =5 pF, VCC = 3.3 V, RS = VCC Gray Scale Pattern	f = 85 MHz	58	64	mA
			f = 135 MHz	70	76	mA
		R <sub>L</sub> = 100Ω, C <sub>L</sub> =5 pF, VCC = 3.3 V, RS = GND Gray Scale Pattern	f = 85 MHz	44	50	mA
			f = 135 MHz	56	62	mA
Transmitter Supply Current	I <sub>TCCW</sub>	R <sub>L</sub> = 100Ω, C <sub>L</sub> = 5 pF, VCC = 3.3 V, RS = VCC Worst Case Pattern	f = 85 MHz	69	75	mA
			f = 135 MHz	87	93	mA
		R <sub>L</sub> = 100Ω, C <sub>L</sub> = 5 pF, VCC = 3.3 V, RS = GND Worst Case Pattern	f = 85 MHz	55	61	mA
			f = 135 MHz	73	79	mA
Transmitter Power Down Supply Current	I <sub>TCCS</sub>	/PWDN = L			10	μA

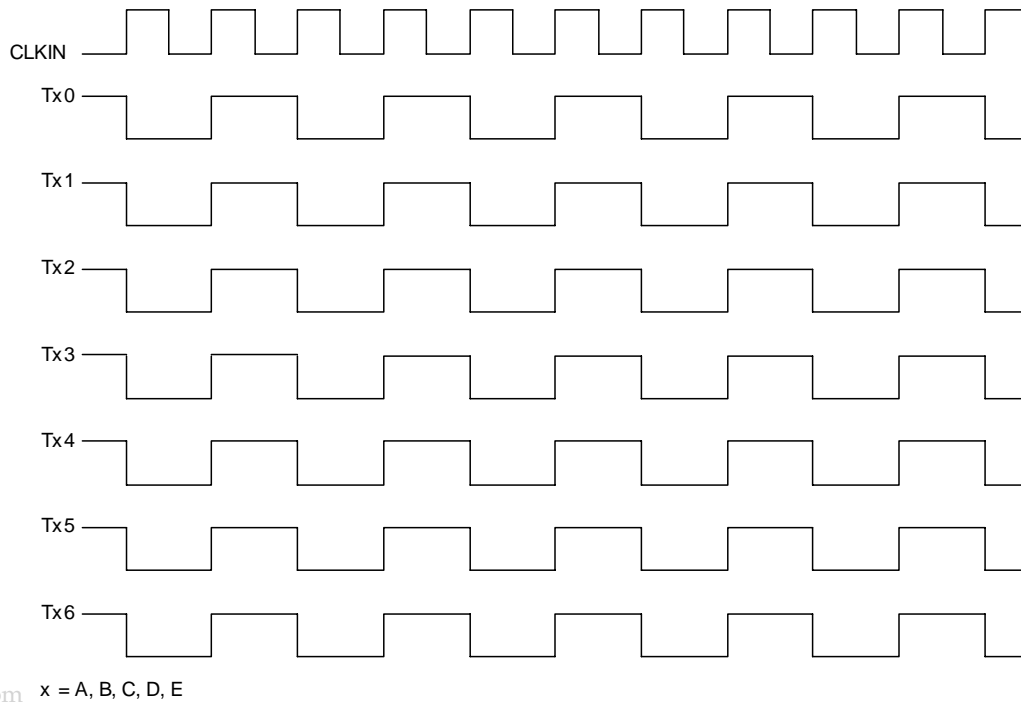




### Gray Scale Pattern



### Worst Case Pattern



[www.DataSheet4U.com](http://www.DataSheet4U.com) x = A, B, C, D, E

## AC Electrical Characteristics





VDD=3.3 V ±10%, Ambient temperature 0 to +70°C

Parameter	Symbol	Min.	Typ.	Max.	Units
<b>Switching Characteristics</b>					
CLK IN Transition Time	t <sub>TCIT</sub>			5	ns
CLK IN Period	t <sub>TCP</sub>	7.4		125.0	ns
CLK IN High Time	t <sub>TCH</sub>	0.35t <sub>TCP</sub>	0.5t <sub>TCP</sub>	0.65t <sub>TCP</sub>	ns
CLK IN Low Time	t <sub>TCL</sub>	0.35t <sub>TCP</sub>	0.5t <sub>TCP</sub>	0.65t <sub>TCP</sub>	ns
CLK IN to TCLK± Delay	t <sub>TCD</sub>		3t <sub>TCP</sub>		ns
TTL Data Setup to CLK IN	t <sub>TS</sub>	2.5			ns
TTL Data Hold from CLK IN	t <sub>TH</sub>	0			ns
LVDS Transition Time	t <sub>LVT</sub>		0.6	1.5	ns
Output Data Position0	t <sub>TOP1</sub>	-0.2	0.0	0.2	ns
Output Data Position1	t <sub>TOP0</sub>	$\frac{t_{TCP}}{7} - 0.2$	$\frac{t_{TCP}}{7}$	$\frac{t_{TCP}}{7} + 0.2$	ns
Output Data Position2	t <sub>TOP6</sub>	$2 \frac{t_{TCP}}{7} - 0.2$	$2 \frac{t_{TCP}}{7}$	$2 \frac{t_{TCP}}{7} + 0.2$	ns
Output Data Position3	t <sub>TOP5</sub>	$3 \frac{t_{TCP}}{7} - 0.2$	$3 \frac{t_{TCP}}{7}$	$3 \frac{t_{TCP}}{7} + 0.2$	ns
Output Data Position4	t <sub>TOP4</sub>	$4 \frac{t_{TCP}}{7} - 0.2$	$4 \frac{t_{TCP}}{7}$	$4 \frac{t_{TCP}}{7} + 0.2$	ns
Output Data Position5	t <sub>TOP3</sub>	$5 \frac{t_{TCP}}{7} - 0.2$	$5 \frac{t_{TCP}}{7}$	$5 \frac{t_{TCP}}{7} + 0.2$	ns
Output Data Position6	t <sub>TOP2</sub>	$6 \frac{t_{TCP}}{7} - 0.2$	$6 \frac{t_{TCP}}{7}$	$6 \frac{t_{TCP}}{7} + 0.2$	ns
Phase Lock Loop Set	t <sub>TPLL</sub>			10.0	ms

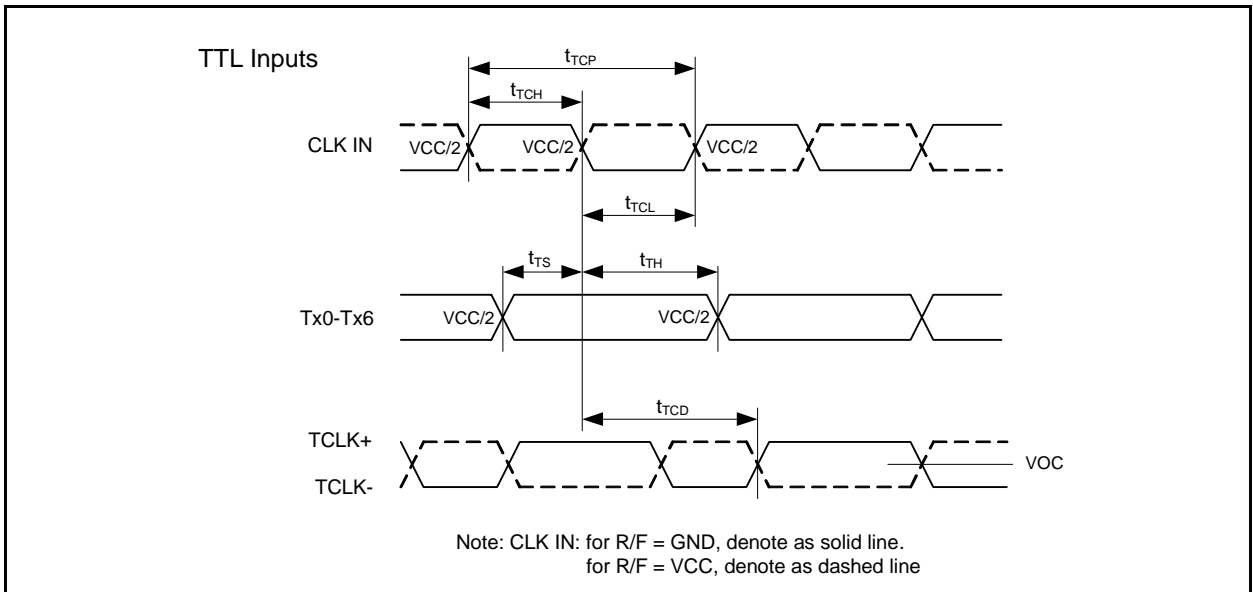
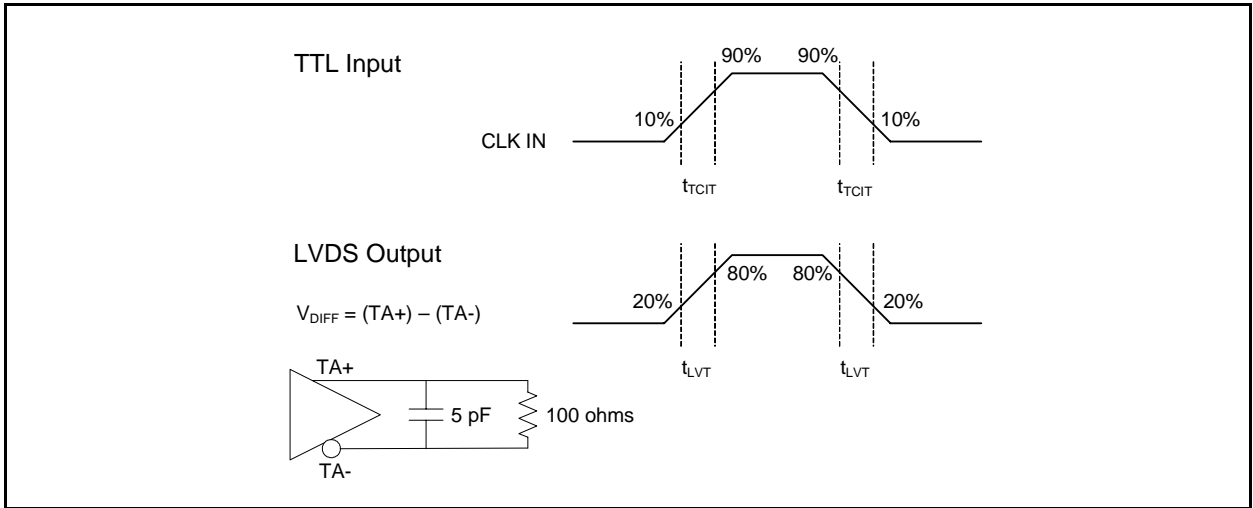
## Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ <sub>JA</sub>	Still air		53		°C/W
	θ <sub>JA</sub>	1 m/s air flow		40		°C/W
	θ <sub>JA</sub>	3 m/s air flow		33		°C/W
Thermal Resistance Junction to Case	θ <sub>JC</sub>			8		°C/W





## AC Timing Diagrams

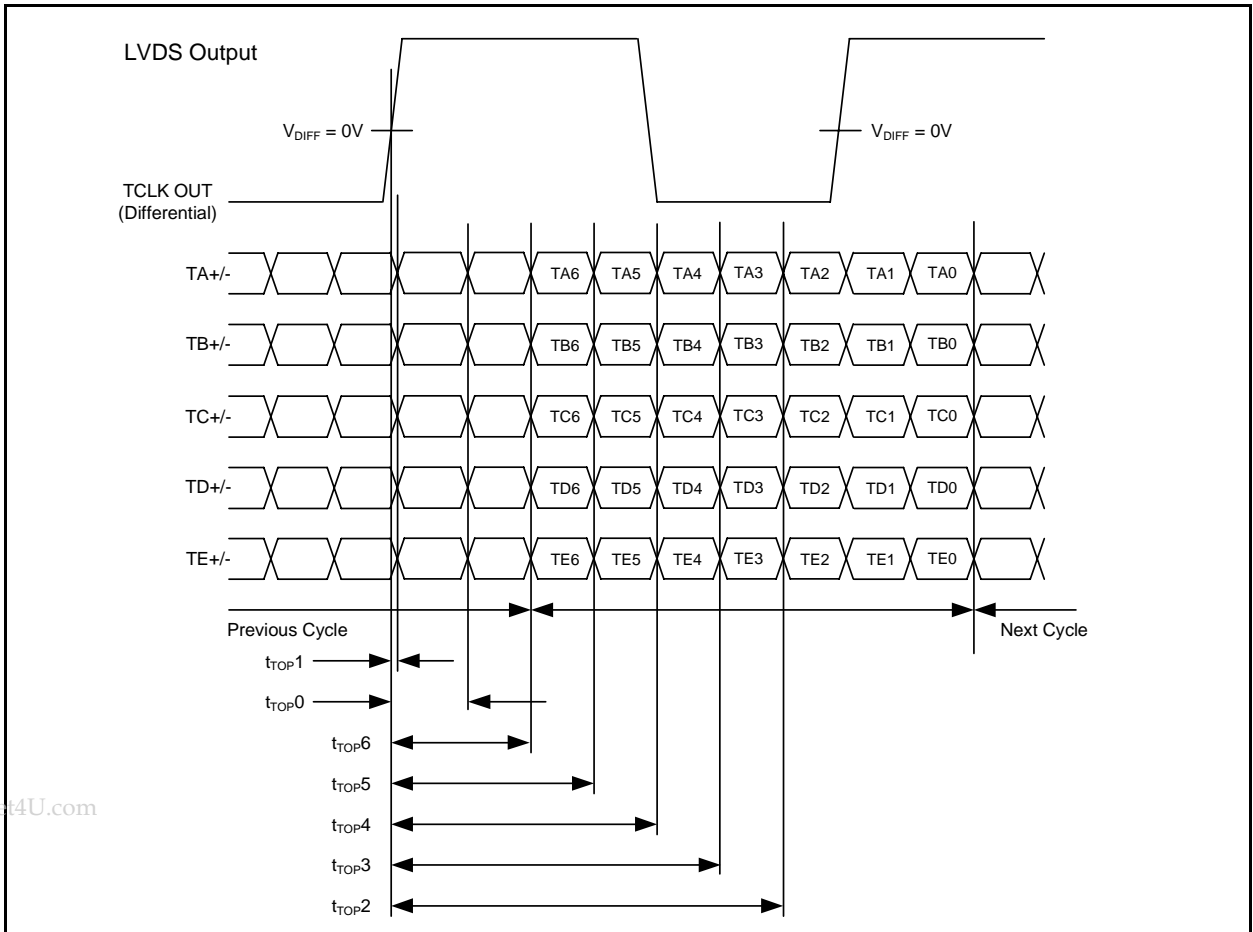
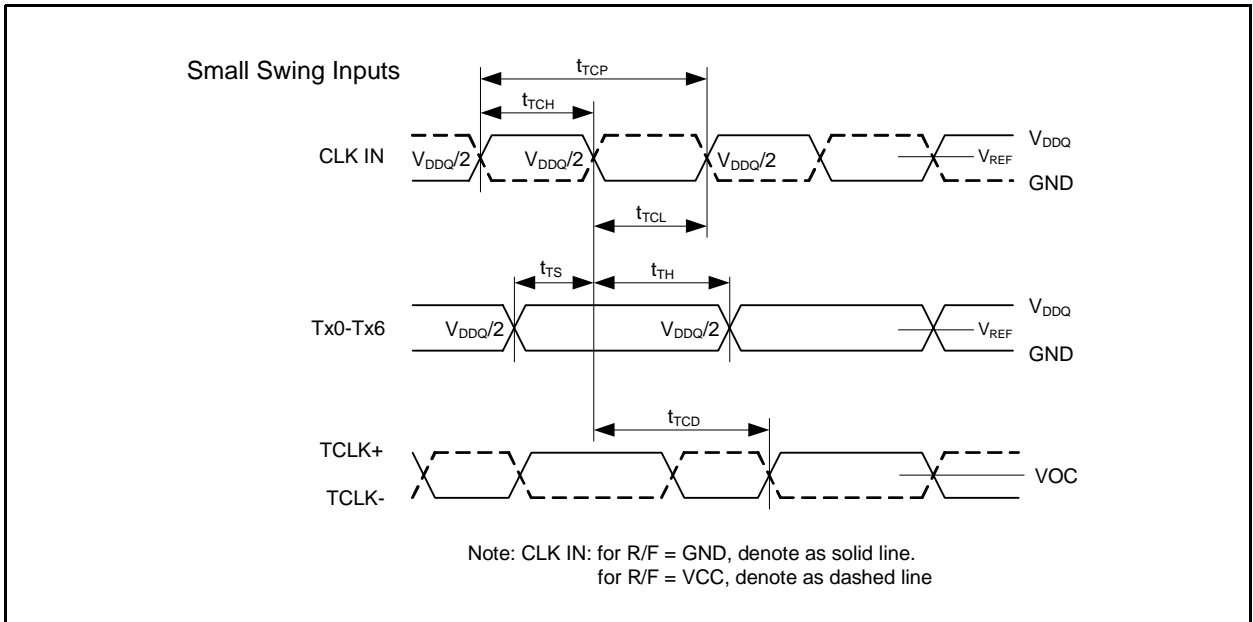






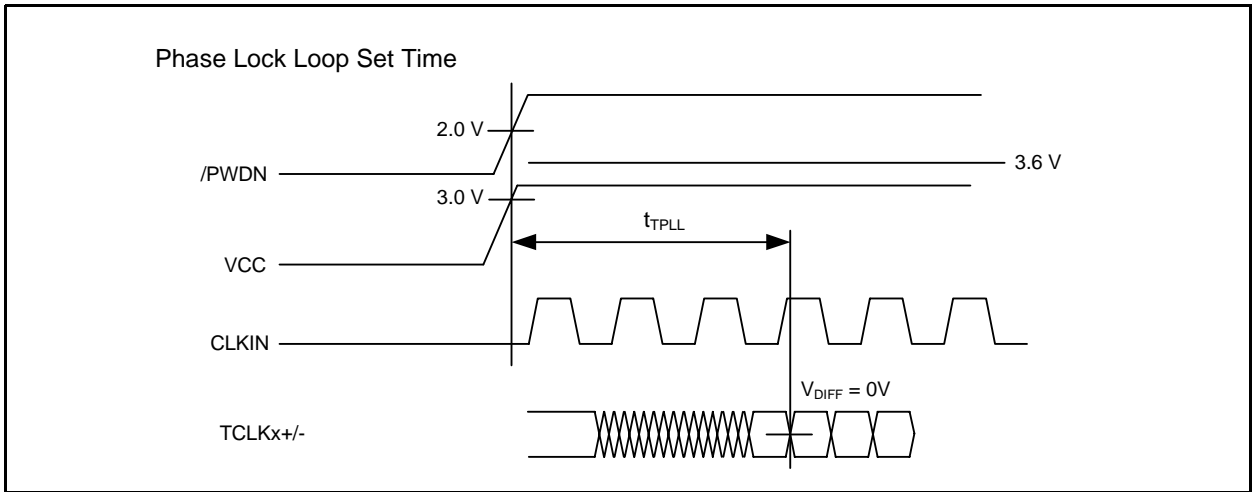
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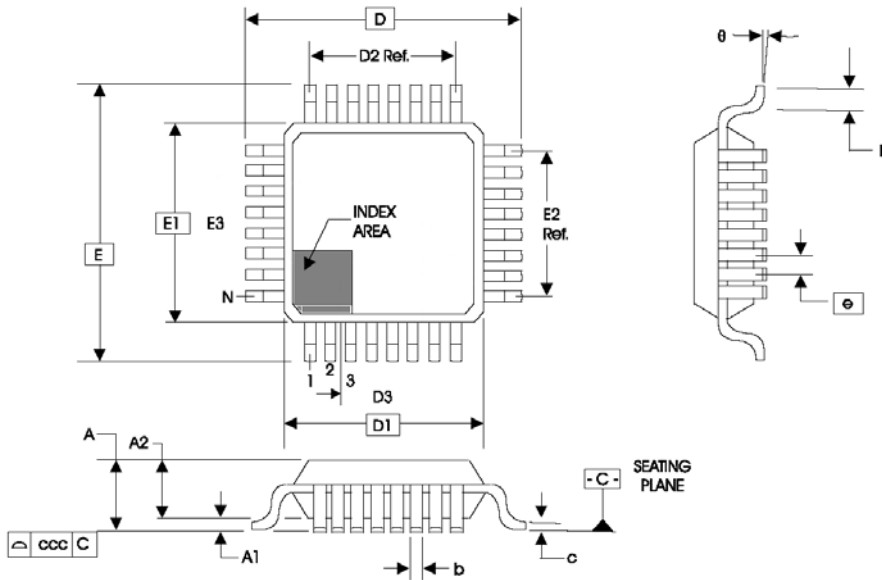






## Package Outline and Package Dimensions (64-pin TQFP)

Package dimensions are kept current with JEDEC Publication No. 95, variation ACD.



ALL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MIN/MAX
N	64
A	-- / 1.20
A1	0.05 / 0.15
A2	0.95 / 1.05
b	0.17 / 0.27
c	0.09 / 0.20
D	12.00 BASIC
D1	10.00 BASIC
D2	7.50 Ref.
E	12.00 BASIC
E1	10.00 BASIC
E2	7.50 Ref.
e	0.50 BASIC
L	0.45 / 0.75
theta	0° / 7°
ccc	-- / 0.08
D3&E3	-

## Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
V103YLF	V103YLF	Tray (160 units per tray)	64-pin TQFP	0 to +70° C
V103YLFT	V103YLF	Tape and Reel	64-pin TQFP	0 to +70° C

The "LF" part number suffix denotes the device as Lead (Pb) Free and that the device is RoHS compliant.

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